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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/510,894	PERDUE, KENNETH LEE	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Re: Rejection of claims 1-4 and 14-15

Applicant asserts that, "the foregoing allegations and cited passage of DeVos do not anticipate or render obvious independent claims 1 and 15. First, Applicant points out that the cited passage of DeVos (column 4, lines 51-62) simply states:

"A software program for write-in operation is down-loaded from the system manager 60 to the RAM 24 of the SMU 20 before copy operation of the video data is performed. The CPU 22 of the SMU 20 controls write-in operation of the physical storage medium, 21 according to the software program for write-in operation stored in the RAM 24. Then the software program for write-in operation in the RAM 24 is replaced with a software program for read-out operation by down-load from the system manager 60 before video service starts. The CPU 22 controls read-out operation of the physical storage medium 21 according to the software program for read-out operation in video service."

As indicated above, the cited passage of DeVos nowhere states that CPU 22 (the alleged "control circuit" of claim 1) inhibits signals transmitted from the output line of physical storage medium 21 (the alleged "second circuit" of claim 1) to the input line of ATM interface 29 (the alleged "first circuit" of claim 1) when ATM interface 29 is

transmitting signals to the input line of physical storage medium 21. Rather, the cited passagee of DeVos is completely silent regarding the signal transmission capabilities of physical storage medium 21 when ATM interface 29 is transmitting signals to physical storage medium 21. Accordingly, the Examiner's bald allegation that "[d]uring write-in operations, element 21 is not allowed to transmit any data" (see discussion of claim 3 on page 4 of Office Action dated December 13, 2006) is completely without support".

The examiner respectfully disagrees. When the software for write-in is replaced with the software program for read-out the CPU 22 controls read-out operation of element 21. Meaning that, if CPU controls write-in and read-out operation of element 21, it is inherent that when operating in write-in operation the read-out operation is disabled, thus, inhibiting any signals from coming in when 21 is transmitting signals, and vice versa. However, taking the contrary, the examiner has issue new ground of rejections to substantiate for the "inhibiting" limitation.

Re: Rejection of claims 5-8, 10, 12-13 and 16-18

See new ground of rejections. Furthermore, the two references, as a whole, meet these limitations.

Re: Rejection of claims 8-9 and 19-20

See new ground of rejections. Furthermore, the two references, as a whole, meet these limitations.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims (1-2, 4-20) are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, and in view of Sgambati (US Patent 5,606,443).**

Re claim 1, Applicant's admitted prior art discloses a circuit arrangement comprising: a first circuit having an output line and an input line (See fig. 1: 12); a second circuit having an input line for receiving signals from the output line of the first circuit, and an output line for transmitting signals to the input line of the first circuit (See fig. 1: 10).

But applicant's admitted prior art fails to teach a control circuit for controlling signals transmitted from the output line of the second circuit to the input line of the first circuit by inhibiting the signals transmitted from the output line of the second circuit to

the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit.

However, Sgambati does. (See fig. 1: 10 & fig. 4A & B, col. 6, lines 15-35) Sgambati discloses a controller for controlling signas received by the IR receiver to be sent to the IR transmitter. This is accomplished by an output line which enables or disable the repeater function of the controller. When the ouput line is logic 1 (high state) signals received through a jack (146), signals received by the IR receiver and which are sent by the IR receiver to the controller, are inhibited from passage through NOR gate.

Therefore, taking the combined teachings of applicant's admitted prior art and Sgambati as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated a controller into the system of applicant's admitted prior art, in the manner as claimed, and as taught by Sgambati, for the benefit of enabling/disabling the repeater function (retransmission) of the controller. (See col. 6, lines 29-30 & col. 9, lines 23-28)

Re claim 2, the combination of applicant's admitted prior art and Sgambati further disclose that wherein the circuit arrangement is included in a television receiver.(In Sgambati, see fig. 1 & col. 3, lines 31-40. Furthermore, this circuit arrangement has been used in the ATC311 high definition televisions as disclosed by the applicant in paragraph 17.)

Re claim 4, the combination of applicant's admitted prior art and Sgambati further disclose that, wherein the control circuit keeps the input line of the first circuit at a high state when the first circuit is transmitting signals to the input line of the second circuit. (In Sgambati, see fig. 1. One skilled in the art would know that the input line of the first circuit must be kept high state (logic 1) when transmitting to the IR receiver, that way no signal are inputted to the first circuit.)

Re claim 5, the combination of applicant's admitted prior art and Sgambati further disclose that wherein the first circuit is a selected one of Universal Asynchronous Receiver/Transmitter (UART) and a Universal Synchronous/Asynchronous Receiver/Transmitter (USART). (In applicant's admitted prior art, see fig. 1)

Re claim 6, the combination of applicant's admitted prior art and Sgambati further disclose that, wherein the second circuit is a G-Link circuit. (In applicant's admitted prior art, see fig. 1)

Re claim 7, the combination of applicant's admitted prior art and Sgambati further disclose that wherein the second circuit further comprises a bi-directional line. (In applicant's admitted prior art, see fig. 1)

Re claim 8, the combination of applicant's admitted prior art and Sgambati further disclose that, wherein short-circuiting the bidirectional line initiates a demonstration

mode. (In applicant's admitted prior art, see fig. 1 & paragraph 5. One skilled in the art would know that short-circuiting would cause the initiation of a demonstration mode.)

Re claim 9, the combination of applicant's admitted prior art and Sgambati further disclose that wherein the shorting circuiting is a short circuit to ground. (One skilled in the art would know that shorting the circuit to ground is one way short circuiting is accomplished.)

Re claim 10, the combination of applicant's admitted prior art and Sgambati further disclose that wherein the first circuit generates an interrupt signal if the first circuit receives the signals transmitted from the second circuit. (In applicant's admitted prior art, see paragraphs 4-5)

Re claim 11, the combination of applicant's admitted prior art and Sgambati further disclose that, wherein signals transmitted from the output line of the first circuit control an external pager module through the second circuit for connecting to a pager service. (In applicant's admitted prior art, see paragraphs 4-5. One skilled in the art would know that G-link circuits can be connected to control external pager module. Furthermore, this circuit arrangement has been used in the ATC311 high definition televisions as disclosed by the applicant in paragraph 17.)

Re claim 12, the combination of applicant's admitted prior art and Sgambati further disclose that, wherein the second circuit further comprises a second input line for receiving IR signals transmitted from an IR source and a second output line for transmitting the IR signals for remotely controlling an external device. (In applicant's admitted prior art, see paragraphs 4-5)

Re claim 13, the combination of applicant's admitted prior art and Sgambati further disclose that, wherein the second circuit provides feedback between the output line of the first circuit and the input line of the first circuit. (In applicant's admitted prior art, see paragraphs 4-5)

Re claim 14, the combination of applicant's admitted prior art and Sgambati further disclose that wherein the control circuit controls the signals transmitted from the output line of the second circuit to the input line of the first circuit according to a mode of operation. (See fig. 1: 10 & fig. 4A & B, col. 6, lines 15-35.)

Claim 15 is a method claim corresponding to system claim 1. Hence, the elements in system claim 1 would have necessitated the steps performed in method claim 15. Therefore, claim 15 has been analyzed and rejected w/r to claim 1 above.

Claim 16 is a method claim corresponding to system claim 5. Hence, the elements in system claim 5 would have necessitated the steps performed in method

claim 16. Therefore, claim 16 has been analyzed and rejected w/r to claim 5 above.

Claim 17 is a method claim corresponding to system claim 6. Hence, the elements in system claim 6 would have necessitated the steps performed in method claim 17. Therefore, claim 17 has been analyzed and rejected w/r to claim 6 above.

Claim 18 is a method claim corresponding to system claim 7. Hence, the elements in system claim 7 would have necessitated the steps performed in method claim 18. Therefore, claim 18 has been analyzed and rejected w/r to claim 7 above.

Claim 19 is a method claim corresponding to system claim 8. Hence, the elements in system claim 8 would have necessitated the steps performed in method claim 19. Therefore, claim 19 has been analyzed and rejected w/r to claim 8 above.

Claim 20 is a method claim corresponding to system claim 9. Hence, the elements in system claim 9 would have necessitated the steps performed in method claim 20. Therefore, claim 20 has been analyzed and rejected w/r to claim 9 above.

5. **Claims (1 & 15) are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, in view of Park (KR 20010661358).**

Re claim 1, Applicant's admitted prior art discloses a circuit arrangement comprising: a first circuit having an output line and an input line (See fig. 1: 12); a

second circuit having an input line for receiving signals from the output line of the first circuit, and an output line for transmitting signals to the input line of the first circuit (See fig. 1: 10).

But applicant's admitted prior art fails to teach a control circuit for controlling signals transmitted from the output line of the second circuit to the input line of the first circuit by inhibiting the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit.

However, Park does. (See abstract) Park discloses a half-duplex communication control circuit which blocks reception data in case of transmission and prevents transmission data in case of reception.

Therefore, taking the combined teachings of applicant's admitted prior art and Park as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated a half-duplex control circuit into the system of applicant's admitted prior art, in the manner as claimed, and as taught by Park, for the benefit of allowing serial infrared communication to be stably carried out. (See abstract)

Claim 15 is a method claim corresponding to system claim 1. Hence, the elements in system claim 1 would have necessitated the steps performed in method claim 15. Therefore, claim 15 has been analyzed and rejected w/r to claim 1 above.

6. **Claims (1 & 15) are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, in view of De Vos et al (hereinafter De Vos) (US Patent 6,367,079 B1).**

Re claim 1, Applicant's admitted prior art discloses a circuit arrangement comprising: a first circuit having an output line and an input line (See fig. 1: 12); a second circuit having an input line for receiving signals from the output line of the first circuit, and an output line for transmitting signals to the input line of the first circuit (See fig. 1: 10).

But applicant's admitted prior art fails to teach a control circuit for controlling signals transmitted from the output line of the second circuit to the input line of the first circuit by inhibiting the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit.

However, De Vos does. (See fig. 2A or 4A: 22 & col. 4, lines 51-62.) De Vos discloses a control circuit (22) for controlling signals transmitted from the output line of the second circuit (29) to the input line of the first circuit (21) by inhibiting the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit. When the software for write-in is replaced with the software program for read-out the CPU 22 controls read-out operation of element 21. Meaning that, if CPU controls write-in and read-out operation of element 21, it is inherent that when operating in write-in operation

the read-out operation is disabled, thus, inhibiting any signals from coming out when 21 is transmitting signals, and vice versa.

Therefore, taking the combined teachings of applicant's admitted prior art and De Vos as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated a CPU control circuit into the system of applicant's admitted prior art, in the manner as claimed, and as taught by De Vos, for the benefit of controlling write-in and read-out operation. (See col. 4, lines 51-62)

Claim 15 is a method claim corresponding to system claim 1. Hence, the elements in system claim 1 would have necessitated the steps performed in method claim 15. Therefore, claim 15 has been analyzed and rejected w/r to claim 1 above.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
April 14, 2007

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER